

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:
  - a first impurity region of a first conductivity type formed on a main surface of a semiconductor substrate;
  - a first isolating insulation film formed on a surface of said first impurity region;
  - a second impurity region of a second conductivity type formed at that portion of said first impurity region which is positioned immediately below said first isolating insulation film;
  - a third impurity region of the second conductivity type formed at a surface of a portion of said first impurity region, spaced apart from said first isolating insulation film;
  - a fourth impurity region of the second conductivity type formed on a portion of said first impurity region on a side opposite to said third impurity region with said first isolating insulation film positioned therebetween, spaced apart from said first isolating insulation film;
  - a first electrode portion formed on that portion of said first impurity region which is sandwiched between said second impurity region and said third impurity region; and
  - a second electrode portion formed on that portion of said first impurity region which is sandwiched between said second impurity region and said fourth impurity region.

2. The semiconductor device according to claim 1, comprising:
  - a second isolating insulation film formed spaced apart from said first isolating insulation film, at a surface of that portion of said first impurity region which is on a side where said third impurity region is positioned, with respect to said first isolating insulation film; and
  - a third isolating insulation film formed spaced apart from said first isolating insulation film, at a surface of that portion of said first impurity region which is on a side where said fourth impurity region is positioned, with respect to said first isolating insulation film; wherein

10           said third impurity region includes  
          a first concentration region having a prescribed impurity  
concentration formed at that portion of said first impurity region which is  
positioned immediately below said second isolating insulation film, and  
          a second concentration region having an impurity concentration  
15       higher than said first concentration region, electrically connected to said  
first concentration region and formed in a direction away from said first  
isolating insulation film with respect to said second isolating insulation  
film; and  
          said fourth impurity region includes  
20       a third concentration region having a prescribed concentration  
formed at that portion of said first impurity region which is positioned  
immediately below said third isolating insulation film, and  
          a fourth concentration region having an impurity concentration  
higher than said third concentration region, electrically connected to said  
25       third concentration region and formed in a direction away from said first  
isolating insulation film with respect to said third isolating insulation film.

3. The semiconductor device according to claim 2, wherein  
said second impurity region, said third impurity region and said  
fourth impurity region are each formed as wells.

4. The semiconductor device according to claim 2, wherein  
said first electrode portion and said second electrode portion are  
formed to traverse a surface of said first impurity region, respectively;  
in a first channel region positioned immediately below said first  
5       electrode portion, channel width corresponding to length of a portion of said  
first electrode portion traversing the surface of said first impurity region is  
set shorter than channel width corresponding to length of said second  
electrode portion traversing the surface of said first impurity region, in a  
second channel region positioned immediately below said second electrode  
10       portion; and  
          in said second impurity region, width along a direction of extension

15 of said first electrode portion and said second electrode portion in said second impurity region changes smoothly from a portion positioned on the side of said first channel region to a portion positioned on the side of said second channel portion.

5 5. The semiconductor device according to claim 2, wherein said first electrode portion and said second electrode portion are formed to traverse a surface of said first impurity region, respectively; channel width of said first channel region corresponding to length of a portion of said first electrode portion traversing the surface of said first impurity region is set shorter than channel width of said second channel region corresponding to length of said second electrode portion traversing the surface of said first impurity region; 10 in said second impurity region, a portion is provided of which width along a direction of extension of said first electrode portion and said second electrode portion in said second impurity region changes steeply from a portion positioned on the side of said first channel region to a portion positioned on the side of said second channel region; and 15 said second electrode portion is formed to cover said steeply changing portion.

6. The semiconductor device according to claim 1, wherein said second impurity region, said third impurity region and said fourth impurity region are each formed as wells.

5 7. The semiconductor device according to claim 1, wherein said first electrode portion and said second electrode portion are formed to traverse a surface of said first impurity region, respectively; in a first channel region positioned immediately below said first electrode portion, channel width corresponding to length of a portion of said first electrode portion traversing the surface of said first impurity region is set shorter than channel width corresponding to length of said second electrode portion traversing the surface of said first impurity region, in a

second channel region positioned immediately below said second electrode portion; and

in said second impurity region, width along a direction of extension of said first electrode portion and said second electrode portion in said second impurity region changes smoothly from a portion positioned on the side of said first channel region to a portion positioned on the side of said second channel portion.

8. The semiconductor device according to claim 1, wherein said first electrode portion and said second electrode portion are formed to traverse a surface of said first impurity region, respectively; channel width of said first channel region corresponding to length of a portion of said first electrode portion traversing the surface of said first impurity region is set shorter than channel width of said second channel region corresponding to length of said second electrode portion traversing the surface of said first impurity region;

in said second impurity region, a portion is provided of which width along a direction of extension of said first electrode portion and said second electrode portion in said second impurity region changes steeply from a portion positioned on the side of said first channel region to a portion positioned on the side of said second channel region; and

said second electrode portion is formed to cover said steeply changing portion.

9. A semiconductor device, comprising:

a first impurity region of a first conductivity type formed on a main surface of a semiconductor substrate;

an isolating insulation film formed on a surface of said first impurity region;

a second impurity region of a second conductivity type formed at that portion of said first impurity region which is positioned immediately below said isolating insulation film;

a third impurity region of a second conductivity type, electrically

10 connected to said second impurity region and formed at a portion of said  
first impurity region in a direction away from said isolating insulation film;  
a fourth impurity region of the second conductivity type formed  
spaced apart from said isolating insulation film, at a surface of that portion  
of said first impurity region which is opposite to the side where said third  
15 impurity region is positioned; and  
an electrode portion formed on a portion of said first impurity region  
sandwiched by said second impurity region and said fourth impurity  
region; wherein  
in said second impurity region, a portion is formed of which width  
20 along a direction approximately orthogonal to a direction from said  
electrode portion to said third impurity region made narrower, from the  
side of said electrode to the side of said third impurity region.

10. The semiconductor device according to claim 9, wherein said  
width in said second impurity region changes smoothly from the side of  
said electrode portion to the side of said third impurity region.

11. The semiconductor device according to claim 9, wherein said  
electrode portion is formed to cover said portion of said second impurity  
region of which width is changed.

12. The semiconductor device according to claim 9, comprising  
another electrode portion fixed at the same potential as said third impurity  
region and formed on said isolating insulation film to cover said second  
impurity region.